

LH531V00

CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 words × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
 - Operating: 275 mW (MAX.)
 - Standby: 550 μW (MAX.)
- Mask-programmable $\overline{OE}_1/\overline{OE}_1/DC$
- Fully-static operation
- TTL-compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
 - 32-pin, 600-mil DIP
 - 32-pin, 525-mil SOP
 - 32-pin, 8 × 20 mm² TSOP (Type I)

DESCRIPTION

The LH531V00 is a 1M-bit mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

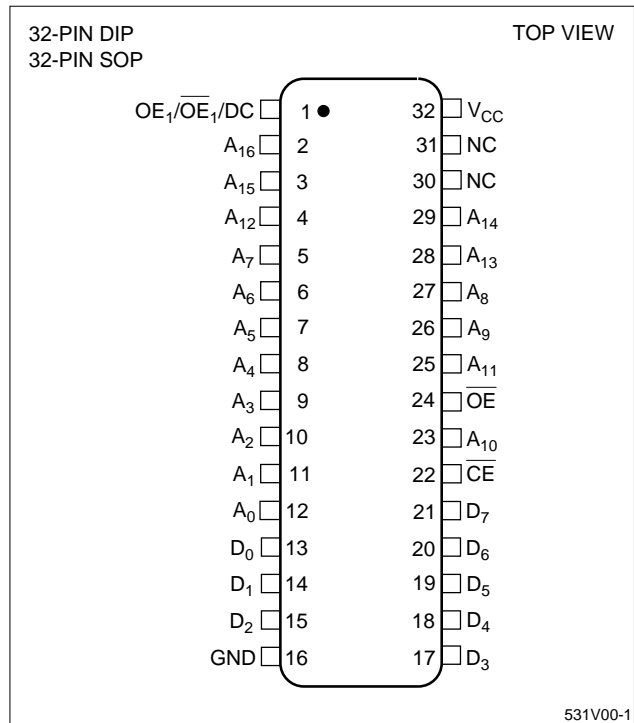


Figure 1. Pin Connections for DIP and SOP Packages

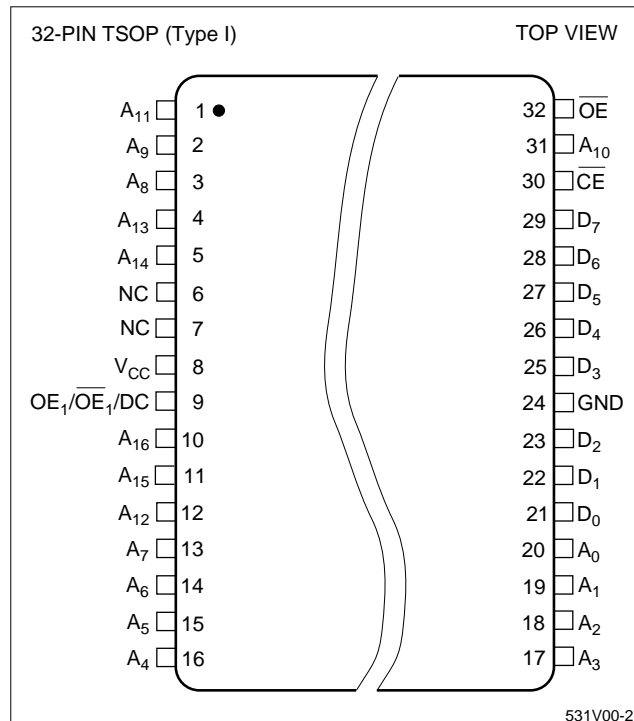


Figure 2. Pin Connections for TSOP Package

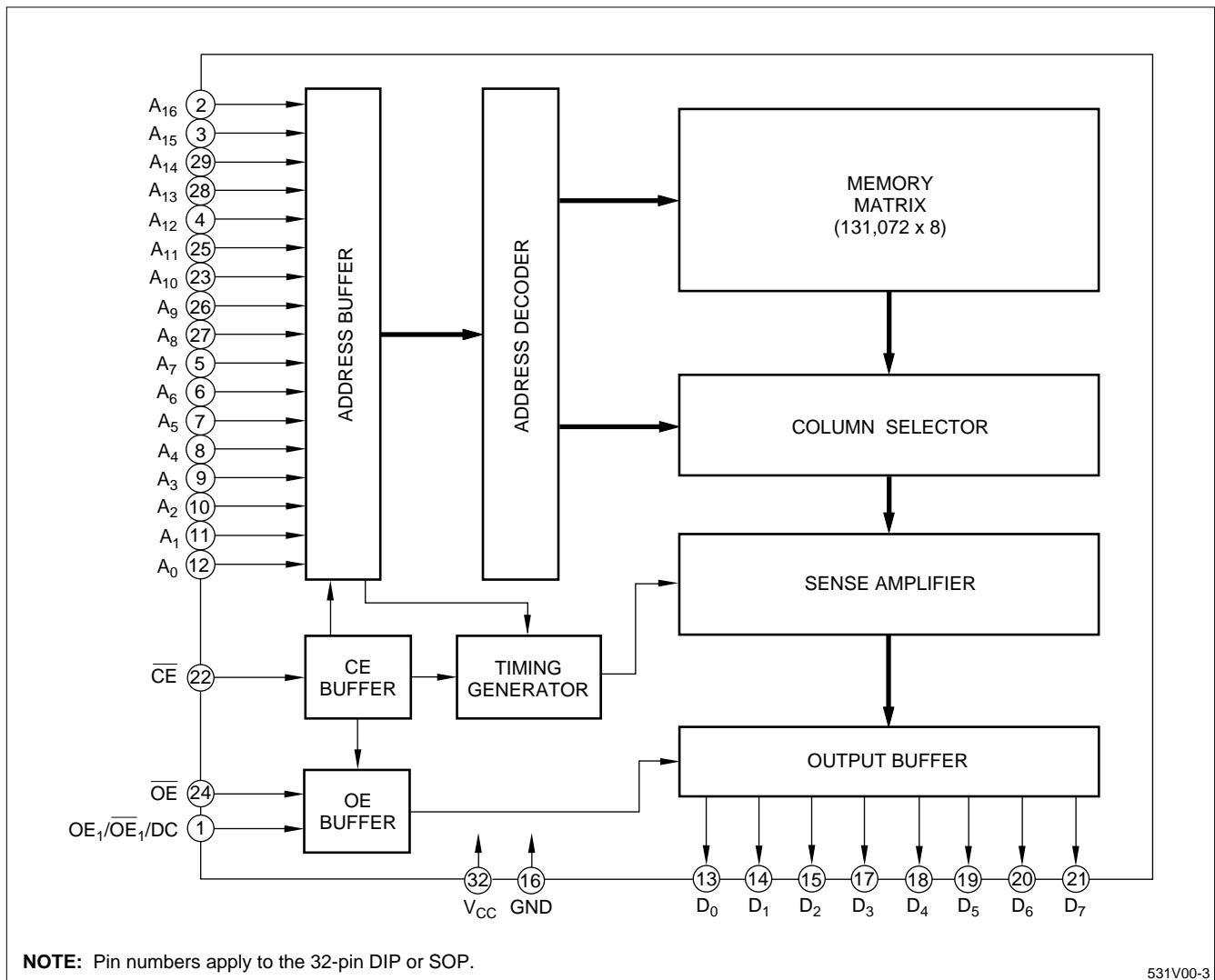


Figure 3. LH531V00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₀ – A ₁₆	Address input	
D ₀ – D ₇	Data output	
\overline{CE}	Chip Enable input	
\overline{OE}	Output Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE_1}/\overline{OE_1}/DC$	Output Enable input	1
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

- Active level of $\overline{OE_1}/\overline{OE_1}/DC$ is mask-programmable. When DC is selected out of $\overline{OE_1}/\overline{OE_1}/DC$, it is fixed to an active level. Then it is recommended to apply either HIGH or LOW to the DC pin.

TRUTH TABLE

\overline{CE}	\overline{OE}	OE_1/\overline{OE}_1	D ₀ – D ₇	SUPPLY CURRENT	NOTE
H	X	X	High-Z	Standby (I _{SB})	1
L	H	X	High-Z	Operating (I _{CC})	1
L	X	L/H	High-Z	Operating (I _{CC})	1
L	L	H/L	D ₀ – D ₇	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		–0.3		0.8	V	
Input 'High' voltage	V _{IH}		2.2		V _{CC} + 0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = 100 ns			50	mA	2
	I _{CC2}	t _{RC} = 1 μs			45	mA	
	I _{CC3}	t _{RC} = 100 ns			45	mA	3
	I _{CC4}	t _{RC} = 1 μs			40	mA	
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$			3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$			100	μA	
Input capacitance	C _{IN}	f = 1 MHz			10	pF	
Output capacitance	C _{OUT}	T _A = 25°C			10	pF	

NOTES:

1. $\overline{CE}/\overline{OE} = V_{IH}$
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE} = 0.2 V$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			50	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			50	ns	1
OE to output in High-Z	t_{OHZ}			50	ns	

NOTE:

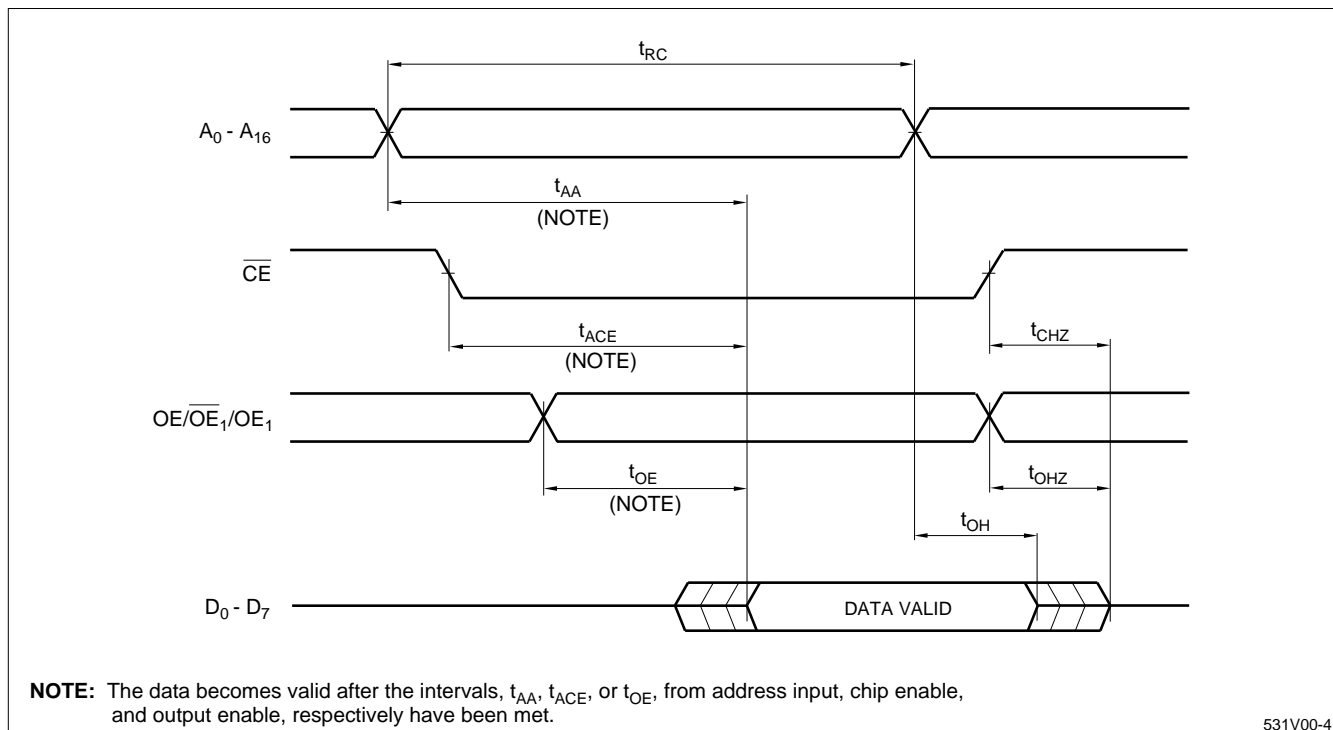
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

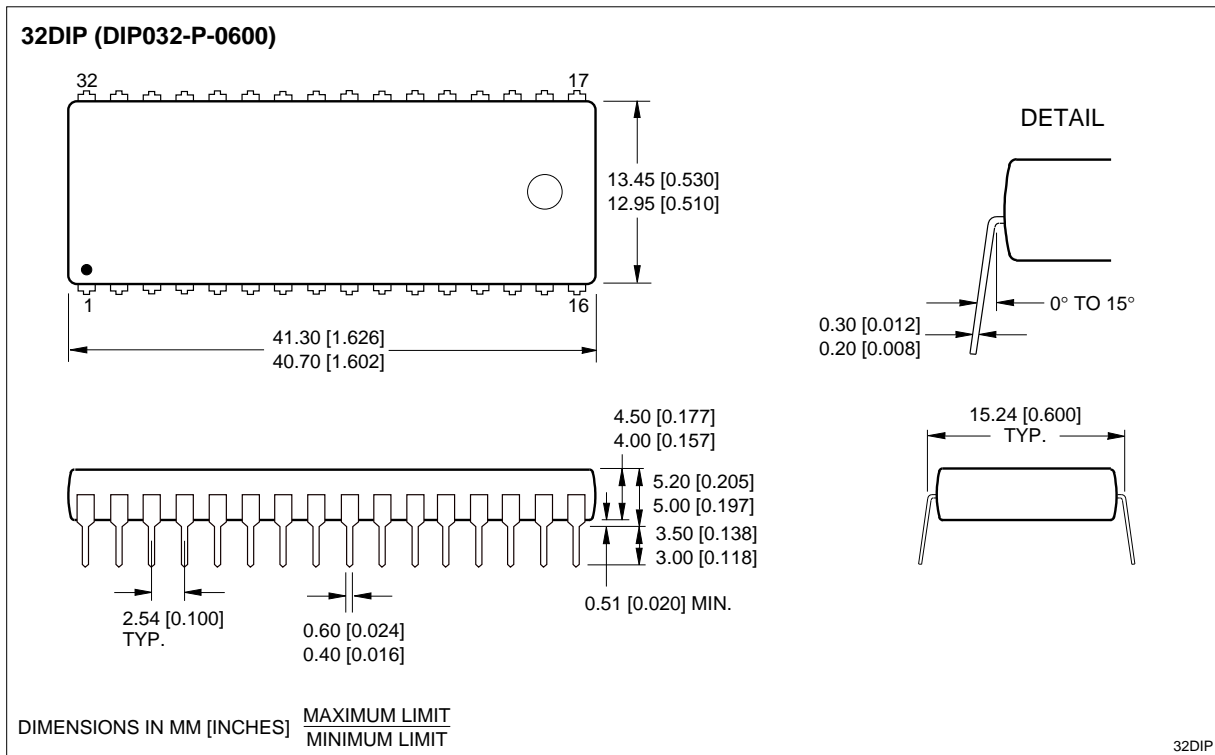
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

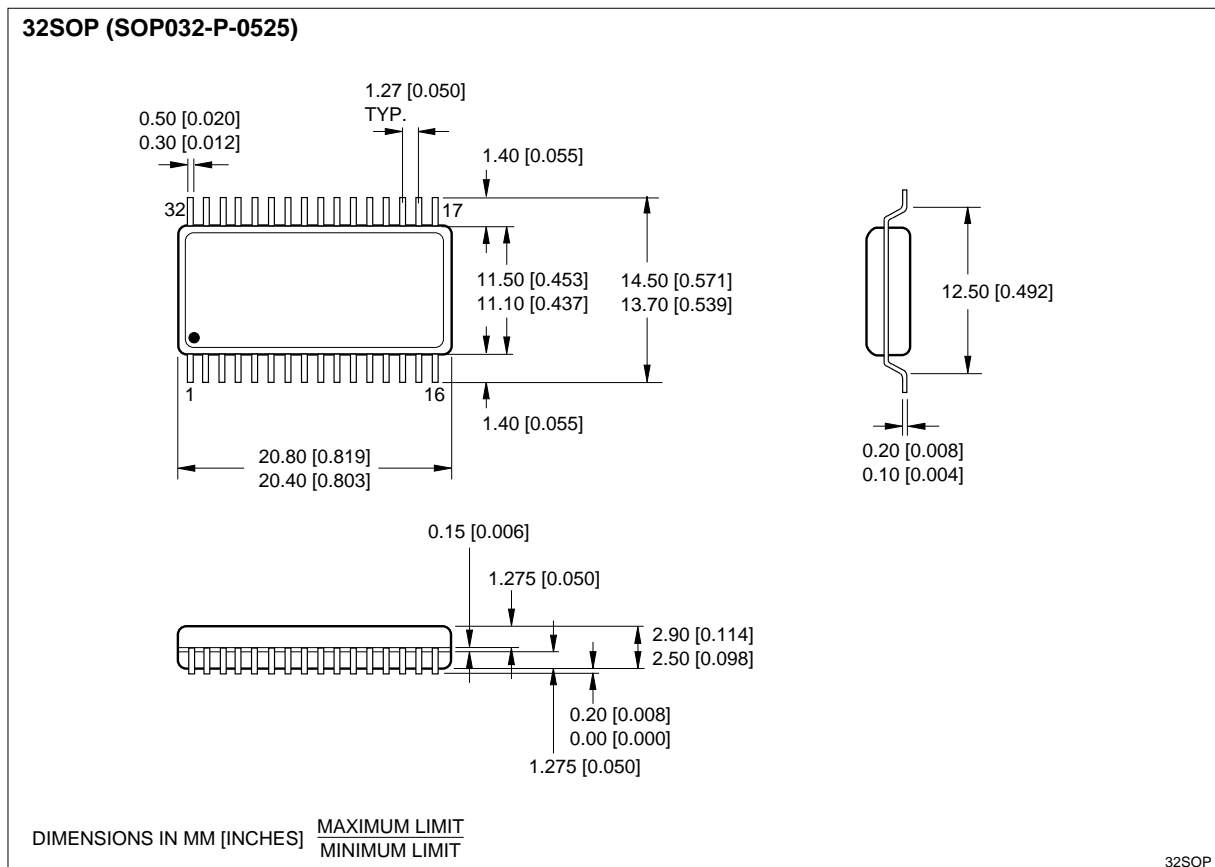
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

**Figure 4. Timing Diagram**

PACKAGE DIAGRAMS

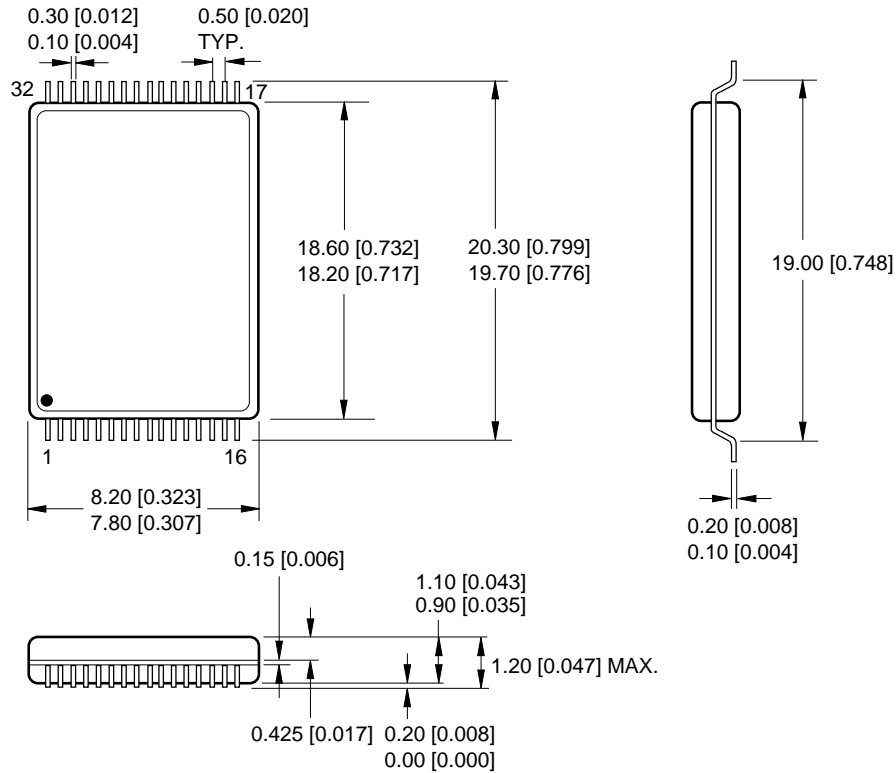


32-pin, 600-mil DIP



32-pin, 525-mil SOP

32TSOP (Type I) (TSOP032-P-0820)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

32TSOP

32-pin, 8 × 20 mm² TSOP (Type I)

ORDERING INFORMATION

LH531V00
Device Type

X
Package

- { D 32-pin, 600-mil DIP (DIP032-P-0600)
- { N 32-pin, 525-mil SOP (SOP032-P-0525)
- { T 32-pin, 8 x 20 mm² TSOP (Type I) (TSOP032-P-0820)

CMOS 1M (128K x 8) Mask-Programmable ROM

Example: LH531V00D (CMOS 1M (128K x 8) Mask-Programmable ROM, 32-pin, 600-mil DIP)

531V00-5